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EXAMINER	
DANG, TRUNG Q	
ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/763,304	SHAJAN MATHEW ET AL.
	Examiner	Art Unit
	Trung Dang	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-28 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14-28 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Chau et al. (US 5,625,217) in view of Nguyen et al. (US 6,084,279 of record).

With reference to Figs 4A-4G, Chau teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer **502** (20-200 Å) on said semiconductor substrate (col. 4, line 9);

forming a conductive layer **504** (sputtered TiN, W, or Co having thickness 20-2,000 Å) on said gate insulator layer (col. 2, line 13; col. 4, lines 14-45);

forming a semiconductor layer **506** (3,500 Å) on said conductive layer (col. 4, lines 53-60);

defining a conductive gate structure and an overlying semiconductor shape, on said gate insulator layer (Fig. 4B);

removing portion of said gate insulator layer not covered by said conductive gate structure (col. 6, lines 16-17);

forming a first doped region **514a/514b** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. 4C and col. 5, lines 27-30);

forming composite insulator spacers on the sides of said conductive gate structure and on the sides of said semiconductor shape (col. 5, lines 43-53);

forming a second doped region **520a/520b** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers (Fig. 4E and col. 6, lines 1-3);

forming a metal layer **522** of Ti or W (Fig. 4F and col. 6, lines 22-24) ;

performing an anneal procedure to form first metal silicide regions **524** from an overlying first portion of said metal layer and from a top portion of said second doped region, and to form a second metal silicide region from an overlying second portion of said metal layer and from a portion of said semiconductor shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers (Fig. 4G and col. 6, lines18-35).

Chau differs from the claims in not disclosing that the metal silicide 524 is formed via total consumption of the polysi semiconductor shape 512.

Nguyen teaches a method in which silicide 85 is formed via total consumption of amorphous silicon or polysilicon gate structure 68 (Figs. 7-8 and col. 5, lines 65-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau's teaching by forming silicide 524 via total consumption of the polysilicon gate 512 as suggested by Nguyen because converting totally the gate electrode 512 to metal silicide would reduce the gate resistance and hence improve the performance of the device

For the limitation of claim 4, see col. 4, lines 20-22 and col. 6, lines 50-57.

3. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. taken with Nguyen as applied to claims 1-4, 6-7, 9 and 13 above, and further in view of Deshpande et al. (US 6,512,266 of record).

The combined process Chau and Nguyen teaches a process for forming a MOSFET device as noted above. The combination differs from the claims in not disclosing a) a high dielectric constant (high-k) material is used for the gate dielectric layer **502** and b) the thickness of the nitride spacer **518a/518b**.

Deshpande teaches a gate dielectric layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). Furthermore, Deshpande teaches the thickness of a nitride spacer of a MOSFET device having LDD regions is typically from about 20 Å to about 1,000 Å (col. 6, lines 9-32).

As for issue a), the subject matter as a whole would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify the combined process by forming the gate dielectric layer **502** using the high-k dielectrics because the substitution of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art.

As for issue b), it would have been obvious to one for ordinary skill in the art to form the nitride spacer in Chau having a thickness suggested by Deshpande because such thickness for a nitride spacer is typical in the art, and utilizing a known value to made the same would have been within the level of one skilled in the art.

4. Claims 1-6, 9-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 5,818,092) in view of Deshpande et al. as cited above.

The rejection is maintained as of record and is repeated herein.

With reference to Figs 2A-2C, Bai teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate dielectric layer **202** on said semiconductor substrate (Fig. 2A);

forming a conductive layer **206** (TiN or TaN) Å) on said gate insulator layer (col. 4, lines 18-19);

forming an amorphous silicon (a-Si) layer **208** (about 500 Å) on said conductive layer (col. 4, lines 33-55);

defining a conductive gate structure and an overlying a-Si shape, on said gate insulator layer (Fig. 2B and col.4, lines 58-64);

removing portion of said gate insulator layer not covered by said conductive gate structure (Fig. 2B);

forming a first doped region **214** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. B and col. 5, lines 1-5);

forming nitride spacers **212** on the sides of said conductive gate structure and on the sides of said a-Si shape (Fig. 2B and col. 5, lines 6-11);

forming a second doped region **216** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said nitride spacers (Fig. 2B and col. 5, lines 11-15);

forming a metal layer **218** of Ti, Co, Pd, Pt, or Ni by sputtering (physical vapor deposition) (Fig. 2B and col. 5, lines 33-60) ;

performing a rapid thermal annealing (RTA) procedure to form first metal silicide regions **220** from an overlying first portion of said metal layer and from a top portion of said second doped region **216**, and to form a second metal silicide region from an overlying second portion of said metal layer and from a portion of said a-Si shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers (Fig. 2C and col. 6, lines 1-58).

For claims 2-4, see col. 5, lines 25-26.

For claim 14, see col. 4, lines 38-39 and col.5, lines 40-41 for the teaching that the a-Si layer **208** is completely or substantially (i.e., not completely) consumed during the silicide reaction.

As for claims 1 and 10, Bai differs from the claims in not disclosing that the nitride spacers **212** are formed of a composite material comprises an oxide liner and a nitride layer. Deshpande teaches a composite insulator spacer comprises an oxide liner 22 and a nitride layer 24, wherein the oxide liner 22 having a thickness of 2 - 400 Å (col. 5, lines 62-65) and the nitride layer having a thickness of 20 - 1,000 Å (col. 6, lines 9-32). It would have been obvious to one for ordinary skill in the art to form the nitride spacer **212** consisting of an oxide liner and a nitride layer having thicknesses as suggested by Deshpande because the oxide liner acts as a buffer to reduce stress generated by the overlying nitride layer and therefore improves insulation between the gate electrode and source/drain regions.

As for claims 5 and 6, Bai differs from the claims in not disclosing that a high dielectric constant (high-k) material is used for the gate dielectric layer **202.** Deshpande teaches a gate dielectric layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). The subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Bai's teaching by forming the gate dielectric layer **202** using the high-k dielectrics because

the selection of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. taken with Deshpande et al. as applied to claims 1-6, 9-14 above, and further in view of Wu (US 6,130,135).

The rejection is maintained as of record and is repeated herein.

The combined process of Bai and Deshpande teaches a method as noted above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. taken with Deshpande et al. as applied to claims 1-6, 9-14 above, and further in view of Tsai et al. (US 2002/0192932 A1) and Wieczorek et al. (US 6,274,511).

The rejection is maintained as of record and is repeated herein.

The combined process of Bai and Deshpande teaches a method as noted

above. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH – H_2SO_4 as claimed. Wieczorek teaches that unreacted refractory metal is removed using typical solution such as HCl:H_2O_2 and H_2SO_4:H_2O_2 (col. 6, lines 37-43; hereinafter solution A). Tsai teaches unreacted refractory metal is removed using a solution such as NH_4OH:H_2O_2 (para. [0026]; hereinafter solution B). Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process of Bai and Deshpande using a mixture comprises HCl:H_2SO_4:NH_4OH:H_2O_2 as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

7. Claims 16-21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. taken with Deshpande et al. as applied to claims 1-6 and 9-14 above, and further in view of Wieczorek et al. as cited above.

The rejection is maintained as of record and is repeated herein.

The combined process of Bai and Deshpande teaches a method as noted above, including the first RTA step to form the silicide layers **220**. The combination differs from the claims in the step of performing a second anneal procedure.

Wieczorek teaches that after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Bai and Wieczorek by performing a second annealing step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claims 25 and 26, see Deshpande, col. 5, line 51 and col. 6, line 17 for the teaching that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art.

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. taken with Deshpande et al. and Wieczorek et al. as applied to claims 16-21 and 24-30 above, and further in view of Wu as cited above.

The rejection is maintained as of record and is repeated herein.

The combined process of Bai taken with Deshpande and Wieczorek teaches a method as noted above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as

suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

9. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. taken with Deshpande et al. and Wieczorek et al. as applied to claims 16-21 and 24-30 above, and further in view of Tsai as cited above.

The rejection is maintained as of record and is repeated herein.

The combined process of Bai taken with Deshpande and Wieczorek teaches a method as noted above, including the teaching of using the aforementioned solution A to remove unreacted refractory metal. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH - H_2SO_4. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above.
Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process using a mixture comprises HCl:H_2SO_4:NH_4OH:H_2O_2 as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

10. Claims 16-22, 24, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (cited above) in view of Nguyen et al. (US 6,084,279 cited by applicants) and Wieczorek et al. (cited above).

Chau teaches a method of forming a MOSFET device as described in the above 102 rejection. Chau differs from the claims in the followings:

a) The gate dielectric layer **502** is of SiO_2 instead of a high-k material as claimed.

b) The semiconductor layer **506** is of polysi instead of amorphous silicon as claimed.

c) The anneal procedure is performed once instead of twice as claimed.

For issues a) and b), Nguyen teaches a method of making a MOSFET device in which the gate dielectric layer **20** is formed from SiO_2, nitrided oxide, or silicon nitride and the top semiconductor layer **68** is of polysi or amorphous silicon (Fig. 6, col. 3, line 1; col. 5, lines 25-27). The subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chau's teaching by replacing SiO_2 with nitride oxide or silicon nitride (high-k materials) for the gate dielectric layer **502** and replacing polysi with amorphous silicon for the semiconductor layer **506** because the substitution of art recognized equivalents as suggested by Nguyen would have been within the level of one skilled in the art.

For issue c), Wieczorek teaches after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Chau and Nguyen by performing a first anneal step using RTA to form metal silicide and then performing a second RTA step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claim 28, see Wieczorek, col. 6, lines 10-15 for the parameters of the first RTA.

11. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen and Wieczorek as applied to claims 16-22, 24, and 28-30 above, and further in view of Wu cited above.

The rejection is maintained as of record and is repeated herein.

The combination of Chau, Nguyen, and Wieczorek teaches a method as described above. The combined process differs from claim in not disclosing that the a-Si layer is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

12. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen and Wieczorek as applied to claims 16-22, 24, and 28-30 above, and further in view of Deshpande et al. cited above.

The rejection is maintained as of record and is repeated herein.

The combination of Chau, Nguyen, and Wieczorek teaches a method as described above. The combined process differs from the claims in not disclosing the thicknesses as well as the means of which the oxide liner and the nitride spacer disclosed in Chau are formed. Deshpande teaches a composite insulator spacer comprises an oxide liner 22 and a nitride layer 24, wherein the oxide liner 22 having a thickness of 2 - 400 Å (col. 5, lines 62-65) and the nitride layer having a thickness of 20 - 1,000 Å (col. 6, lines 9-32). Deshpande in col. 5, line 51 and col. 6, line 17 further teaches that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). It would have been obvious to one for ordinary skill in the art to form, by means of PECVD, the nitride spacer **518a/518b** in Chau consisting of an oxide liner and a nitride layer having thicknesses as suggested by Deshpande because such process parameters are well known in the art of making MOSFET devices, and the application of a known practice to make the same would have been within the level of an artisan. As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art.

13. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen and Wieczorek as applied to claims 16-22, 24, and 28-30 above, and further in view of Tsai et al. cited above.

The rejection is maintained as of record and is repeated herein.

The combination of Chau, Nguyen, and Wieczorek teaches a method as described above, including the teaching of using the aforementioned solution A (see Wieczorek) to remove unreacted refractory metal. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH - H_2SO_4. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above. Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process using a mixture comprises HCl:H_2SO_4:NH_4OH:H_2O_2 as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

Response to Arguments

14. Applicant's arguments filed have been fully considered but they are not persuasive.

With respect to Bai's reference, applicants argue that Bai does not use consumption of silicon layer 208, to protect the subsequent conductive gate structure from a silicide process since the polysilicon gate structure 204, is still separated from the metal silicide by barrier layer 206. This is found unpersuasive because the claims do not exclude barrier layer 206. All that is called for in the claims is a metal silicide layer formed on the conductive gate structure via total consumption of the semiconductor shape. This is exactly taught by Bai, namely metal silicide layer 220 is formed on conductive gate structure 204 via total consumption of the semiconductor shape 208.

For the rejection of claims 16-22, 24, and 28-30 over Chau in view of Nguyen and Wieczorek, applicants do not rebut the Examiner's position even though the combination includes the total consumption of the amorphous silicon in the silicide forming step as pointed out in the rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang

Trung Dang
Primary Examiner
Art Unit 2823

5/2/05